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Title: Selective Control of Test-Access Ports in Integrated Circuits
Assignee: Intel Corporation

REMARKS

Claims 1-2, 4-8, 10, 14-18, 21-22, and 25 are amended, no additional claims are canceled with this response, and no new claims are added; as a result, claims 1-8, 10-25, and 27-28 are now pending in this application.

No new matter has been added by the amendments to claims 1-2, 4-8, 10, 14-18, 21-22, and 25. Support for the amendments to claims 1-2, 4-8, 10, 14-18, 21-22, and 25 is found throughout the specification, including but not limited to the specification at pages 4, line 5 through page 9, line 22, and in Figures 1 and 2.

Objection to the Drawings

The drawings are objected to under 37 C.F.R. § 1.83(a). Specifically, the Office Action states:¹

"The drawings must show every feature of the invention specified in the claims. Therefore, for example: the 'first TAP control device'; the 'second TAP control device'; the 'JTAG boundary-scan controller'; the 'first memory device'; and 'the second memory device'; must be shown or the feature(s) canceled from the claim(s)."

The phrases "first TAP control device" and "second TAP control device" and "JTAG boundary-scan controller" and "first memory device" and "second memory device" have all been deleted from the pending claims in the application.

No amendments to the drawing have been made in response to this objection.

Applicant submits that the claims, at least as now amended, overcome the objection to the drawings, and so respectfully requests withdrawal of the objection.

§112 Rejection of the Claims

Claims 10, 14, 18, and 22.

Claims 10, 14, 18, and 22 (see new claims 29-30 of amendment dated on 6/13/06) were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant traverses the 35 U.S.C. § 112, first paragraph rejection.

¹ See the Office Action at page 2, item 3.

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The specification of the present application at page 4, lines 5-8 states:

Figure 1 shows a block diagram of an exemplary integrated-circuit testing system 100. System 100 includes a test controller 110, an automatic tester 120, Test-Access-Port (TAP) master controller 130, a TAP-control selector 140, and a device under test (DUT) 150.

While Figure 1 illustrates a block diagram of an integrated-circuit testing system, there is no requirement that the blocks of the integrated-circuit testing system 100, as illustrated in Figure 1, be internal to an integrated circuit. This includes no requirements that these blocks be included in any integrated circuit shown as being a device to be tested, such as DUT 150. Therefore, there is no requirement that any one, or any combination, of the test controller 110, the automatic tester 120, the Test-Access-Port (TAP) master controller 130, and the TAP-control selector 140 be "internal of the integrated circuit," as asserted by the Office Action.

As clearly shown in Figure 1, device under test 150, which in various embodiments is an integrated circuit, does not include test controller 110, automatic tester 120, Test-Access-Port (TAP) master controller 130, or TAP-control selector 140. Therefore, the subject matter of each of claims 10, 14, 18, and 22 complies with the requirements of 35 U.S.C. § 112, first paragraph.

Applicant respectfully requests reconsideration and withdrawal of the rejection, and allowance of claims 10, 14, 18, and 22.

Claims 1-8, 14-25 and 27-28.

Claims 1-8, 14-25, and 27-28 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant traverses the 35 U.S.C. § 112, second paragraph rejection.

Claims 1-8, 14-25 and 27-28, at least as now amended, comply with the requirements of 35 U.S.C. § 112, second paragraph. The basis raised in the Office Action for the 35 U.S.C. § 112, second paragraph rejection for each of claims 1-8, 14-25 and 27-28 has been carefully

² See the Office Action at page 3, the fifth sentence in the paragraph under the heading "Claim Rejections - 35 USC § 112 first."

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reviewed, and are believed to have been overcome by the amendments to claims 1-8, 14-25 and 27-28 provided in this response.

Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 112, second paragraph rejection, and allowance of claims 1-8, 14-25, and 27-28.

§103 Rejection of the Claims

Claims 1-8, 25, and 27-28.

Claims 1-8, 25, and 27-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Katzman et al. (U.S. 4.672.535, hereinafter "Katzman") in view of Whetsel (U.S. 6,763,485). Applicant respectfully traverses the rejection of claims 1-8, 25, and 27-28.

Claims 1-8, 25, and 27-28 are not obvious in view of the proposed combination of Katzman and Whetsel³ because the proposed combination of Katzman and Whetsel fails to disclose or suggest all of the subject matter included in any given one of claims 1-8, 25, and 27-28. By way of illustration, independent claim 1, as now amended, includes:

A method comprising:

detecting a condition of an integrated circuit having a testaccess port (TAP) while communicating through a TAP-control selector with the TAP using an automatic tester;

freezing the integrated circuit in a logic state in response to the detected condition;

switching control of the test-access port from the automatic tester to a TAP master controller after freezing the integrated circuit in the logic state; and

communicating through the TAP-control selector with the TAP using the TAP master controller in response to detecting the condition in order to dump state values from the integrated circuit into a memory of the TAP master controller.

In contrast to independent claim 1, Katzman concerns an input/output system for a multiprocessor system.⁴ wherein Katzman recites:⁵

> In a multiprocessor system of the type in which two or more separate processor modules are connected by an

³ Applicant does not admit or agree that any combination of Katzman and Whetsel is possible. ⁴ *See* Katzman at column 3, lines 46-57.

⁵ See Katzman, in the first sentence of the Abstract.

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interprocessor bus dedicated exclusively to interprocessor communication for parallel processing, there is provided an input/output system having multiported device controllers connected to the multiprocessor system by input/output buses.

However, there is no disclosure or suggestion in Katzman of a test-access port, and no disclosure or suggestion in Katzman of "switching control of the test-access port from the automatic tester to a TAP master controller after freezing the integrated eireuit in the logic state," or of "communicating through the TAP-control selector with the TAP using the TAP master controller in response to detecting the condition in order to dump state values from the integrated circuit into a memory of the TAP master controller," all as required by independent claim 1.

The addition of Whetsel fails to disclose or suggest the subject matter of independent elaim 1 as quoted above and missing from Katzman. Therefore, the proposed combination of Katzman and Whetsel fails to disclose or suggest all of the subject matter of independent claim 1, and so independent claim 1 is not obvious in view of the proposed combination of Katzman and Whetsel.

For reasons analogous to those stated above with respect to independent claim 1, the proposed combination of Katzman and Whetsel fails to disclose or suggest all of the subject matter included in independent claims 7 and 25, at least as these claims are now amended.

Claims 2-6, 8, and 27-28 depend from one of independent claims 1, 7, and 25, and therefore include all of the subject matter included in the independent elaim from which they depend, and more. For at least the reasons stated above with respect to independent claims 1, 7, and 25, the proposed combination of Katzman and Whetsel fails to disclose or suggest all of the subject matter included in claims 2-6, 8, and 27-28. Thus, claims 2-6, 8, and 27-28 are not obvious in view of the proposed eombination of Katzman and Whetsel.

Applieant respectfully requests reconsideration and withdrawal of the rejection, and allowance of claims 1-8, 25, and 27-28.

Claims 10-24.

Claims 10-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Whetsel (U.S. 6,763,485). Applicant respectfully traverses the rejection of claims 10-24.

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Applicant believes that it has been established that Whetsel fails to disclose or suggest the subject matter included, for example, in independent claims 1, 7, and 25. For reasons analogous to those stated above with respect to independent claims 1, 7, and 25, Whetsel fails to disclose or suggest all of the subject matter included in any given one of independent claims 10, 14, 18, and 22, at least as these independent claims are now amended. Therefore, independent claims 10, 14, 18, and 22 are not obvious in view of Whetsel.

Claims 11-13, 15-17, 19-21, and 23-24 depend from one of independent claims 10, 14, 18, and 22, and so include all of the subject matter included in the independent claim from which they depend, and more.

For at least the reasons stated above with respect to independent claims 10, 14, 18, and 22. Whetsel fails to disclose or suggest all of the subject matter included in claims 11-13, 15-17, 19-21, and 23-24. Thus, claims 11-13, 15-17, 19-21, and 23-24 are not obvious in view of the Whetsel.

Applicant respectfully requests reconsideration and withdrawal of the rejection, and allowance of claims 10-24.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Serial Number: 10/612,293 Filing Date: June 30, 2003 Title: Selective Control of Test-Access Ports in Integrated Circuits Assignee: Intel Corporation

rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2132 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By Robert B. Madden

Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexendria, VA 22313-1450 on this 2 day of December 2007.

Name

Signature